CLAIMS

Now, therefore, the following is claimed:

1. A computer system for processing instructions of computer programs, comprising:

a register;

a pipeline configured to execute instructions of a computer program, said pipeline having a first stage and a second stage; and

circuitry configured to read a first predicate value from said register and to receive a second predicate value, said circuitry configured to transmit said first predicate value to said first stage and to select one of said predicate values, said circuitry further configured to transmit said selected predicate value to said second stage and to ignore the other one of said predicate values.

2. The system of claim 1, wherein said one predicate value selected by said circuitry is said first predicate value.

3. The system of claim 1, wherein said one predicate value selected by said circuitry is said second predicate value.

4. The system of claim 1, wherein said circuitry is further configured to detect whether an instruction in said second stage is stalled and to select said selected one of said predicate values based on whether said instruction in said second stage is stalled.

5. The system of claim 1, wherein said circuitry includes a latch that transmits said one predicate value selected by said circuitry to said second stage in response to an edge of a clock signal.

6. A computer system, comprising:

a register;

a pipeline configured to execute instructions of a computer program, said pipeline having a first stage and a second stage;

first circuitry coupled to said register and to said first stage, said first circuitry configured to simultaneously receive a first plurality of predicate values, at least one of said first plurality of predicate values received from said register, said first circuitry configured to select one of said first plurality of predicate values, said first circuitry further configured to transmit said selected one of said first plurality of predicate values to said first stage and to transmit said selected one of said first plurality of predicate values across a connection; and

second circuitry coupled to said connection and to said second stage, said second circuitry configured to simultaneously receive a second plurality of predicate values, said second plurality of predicate values including said one predicate value transmitted across said connection, said second circuitry configured to select one of said second plurality of predicate values and to transmit said selected one of said second plurality of predicate values to said second stage.

7. The system of claim 6, wherein said second circuitry includes a latch configured to receive said selected one of said second plurality of predicate values and to transmit said received predicate value in response to an edge of a clock signal.

8. The system of claim 6, wherein one of said second plurality of predicate values is transmitted from another pipeline.

9. The system of claim 6, wherein said second circuitry is further configured to detect whether an instruction in said second stage is stalled and to select said one of said second plurality of predicate values based on whether said instruction is stalled.

10. The system of claim 6, wherein said second circuitry is further configured to simultaneously receive a third plurality of predicate values, said third plurality of predicate values including said selected one of said second plurality of predicate values, said second circuitry configured to select one of said third plurality of predicate values, said second circuitry further configured to transmit said selected one of said third plurality of values to said second stage.

11. The system of claim 6, further comprising control circuitry configured to compare register identifiers defined by said instructions and to transmit control signals to said first and second circuitry, wherein said first circuitry is configured to select said one of said first plurality of predicate values based on at least one of said control signals and said second circuitry is configured to select said one of said second plurality of predicate values based on at least one of said control signals.

12. A method for processing instructions of computer programs, comprising the steps of:

providing a pipeline having a first stage and a second stage;

producing a predicate value;

writing said predicate value to a register;

receiving an instruction;

receiving a control signal;

reading said predicate value from said register based on a register identifier included in said instruction;

transmitting said predicate value read in said reading step to said first stage of said pipeline;

processing said instruction via said first stage of said pipeline based on said predicate value transmitted to said first stage;

receiving a new predicate value;

selecting, based on said control signal, between said new predicate value and said predicate value read in said reading step;

transmitting said predicate value selected in said selecting step to said second stage of said pipeline; and

processing said instruction via said second stage based on said predicate value selected in said selecting step.

13. The method of claim 12, wherein said one predicate value selected in said selecting step is said predicate value read in said reading step.

14. The method of claim 12, wherein said predicate value selected in said selecting step is said new predicate value, said selecting step further including the step of ignoring said predicate value read in said reading step.

15. The method of claim 12, further comprising the steps of:

detecting whether said instruction is stalled; and

performing said selecting step based on said detecting step.

16. The method of claim 12, further comprising the steps of:

detecting whether said new predicate value is indicative of a predicate status of said instruction; and

performing said selecting step based on said detecting step.

17. The method of claim 12, further comprising the steps of:

receiving a second new predicate value;

selecting between said second new predicate value and said value transmitted to said second circuitry;

detecting that said instruction is stalled; and

performing said selecting between said second new predicate value step in response to said detecting step.

18. A method for processing instructions of computer programs, comprising the steps of:

providing a pipeline having a first stage and a second stage;

reading a predicate value from a register;

simultaneously receiving a first plurality of predicate values, said first plurality of predicate values including said predicate value read from said register;

selecting one of said first plurality of predicate values;

transmitting said predicate value selected in said selecting one of said first plurality of predicate values step to said first stage of said pipeline;

processing an instruction in said first stage of said pipeline based on said predicate value transmitted to said first stage;

simultaneously receiving a second plurality of predicate values, said second plurality of predicate values including said one predicate value selected in said selecting one of said first plurality of predicate values step;

selecting one of said second plurality of predicate values;

transmitting said predicate value selected in said selecting one of said second plurality of predicate values step to said second stage of said pipeline; and

processing said instruction in said second stage of said pipeline based on said predicate value transmitted to said second stage.

19. The method of claim 18, further comprising the steps of:

simultaneously receiving a third plurality of predicate values, said third plurality of predicate values including said predicate value selected in said selecting one of said second plurality of predicate values step;

selecting one of said third plurality of predicate values;

transmitting said predicate value selected in said selecting one of said third plurality of predicate values step to said second stage of said pipeline; and

processing said instruction in said second stage of said pipeline based on said predicate value selected in said selecting one of said second plurality of predicate values step.

20. The method of claim 18, further comprising the steps of:

detecting whether said instruction is stalled in said second stage; and

performing said selecting one of said second plurality of predicate values step based on said detecting step.